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Self-cooling on power MOSFET using n-type Si wafer

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Abstract. The self-cooling device was developed by combining the commercial n-channel power MOSFET and the copper plating single-crystalline Sb doped n-type silicon wafer in order to improve heat removal or cooling for power devices. The time dependence of the temperature distribution of the self-cooling device was measured to estimate the heat flux both by the thermal conduction and by the Peltier effect. We found that the average temperature of the upper side of the power MOSFET was cooled down about 0.7℃ by the addition of the copper plating n-type Si wafer after 40 minutes despite enlargement of the temperature distribution range. This fact strongly indicates that the copper plating n-type Si wafer is one of the candidate materials for use in self-cooling devices.

Keywords: self-cooling device, power MOSFET, n-type silicon wafer, electrical resistivity, Seebeck coefficient, thermal conductivity, Peltier heat

INTRODUCTION

Silicon semiconductor power devices that include metal oxide semiconductor field effect transistors (MOSFETs), insulated gate bipolar transistors (IGBTs) and central processing units (CPUs) are used in a daily life to give us modern life in the present time. When we use the electrical equipment incorporating these devices, the improvement of heat removal or cooling is one of the most important issues because they will not function correctly if they are operated at temperatures above 423K.

There are three different ways to remove the heat from the power devices. One is to use the fin connected with the power devices. This cooling system uses only the thermal conduction. Usually the size of the fin is larger than that of the power device itself. The second way is to use the Peltier module connected with the large fin and fan for the Peltier heat dissipation. This cooling system uses only the Peltier heat flux. If we use the second way to cool down the power devices, the electric power consumption of the system is increased because the Peltier module, the fan and the power devices need the different DC power supplies for its operation, respectively. This is the one of the reason why the Peltier module is not applied for cooling down the power devices.

The third way is to use the self-cooling device proposed by Yamaguchi *et al*.[1-3] The cooling process uses both the thermal conduction and the Peltier heat flux driven by its self-current in the self-cooling device. The self-cooling device, for example, consists of the n-type thermoelectric material connected to the Drain for a power MOSFET. In this scheme, it is required that thermoelectric materials for the self-cooling device have a high Seebeck coefficient (S), a high electrical conductivity (σ), and a high thermal conductivity (κ) which is different from the requirement for typical thermoelectric materials such as the Peltier module.

Fortunately, it is easy to find the combinations of high electrical conductivity, high Seebeck coefficient and high thermal conductivity for the self-cooling device because the higher thermal conductivity material usually would have higher electrical conductivity. The typical high thermal conductivity materials are, for example, copper (κ=398W/mK), silicon carbide (κ=490W/mK) and silicon (κ=150W/mK). It has been reported, in fact, that the thermal conductivity of single crystal SiC is higher than that of Cu at room temperature.[4] On the other hand, large values of Seebeck coefficient of single crystal Si have been studied in detail.[5] Recent study has suggested the Seebeck coefficient of heavily doped Si exhibits a hump at a carrier concentration of the order of 10^{19} cm^{-3}, while the electrical resistivity decreases linearly with increasing carrier concentration.[6]

Thus, single crystal Si must be one of the candidate materials for use in the self-cooling device. However, it has yet to be shown that a comprehensive understanding of single crystal Si for the self-cooling device is still lacking. The past thermoelectric studies usually try to find the low thermal conductive materials as thermoelectric materials, and many materials were abandoned because of their high thermal conductivities. The aim of this study is to develop the self-cooling device using the n-type Si wafer which is one of the high thermal conductive materials and to estimate the heat flux both by thermal conduction and by Peltier effect in order to improve heat removal or cooling for the power MOSFET.

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EXPERIMENTAL

The self-cooling device consists of the commercial n-channel power MOSFET (IRF1324PbF, International IOR Rectifier, where the static drain-to-source on-resistance is a maximum of 1.5$m\Omega$) and the substrate of single-crystalline Sb doped n-type silicon with (111) orientation which was cut into rectangular specimens of 15mm×30mm with a thickness of 520μm. The surfaces of the n-type (111) Si wafer were coated with 0.1μm of titanium to ensure adhesion and 0.4μm of gold deposited by sputtering. Copper electrodes were fabricated on both Au surfaces with a thickness of about 2μm deposited by copper plating. The chemical composition of the coatings was clearly found to exist by field emission-electron probe x-ray microanalysis (EPMA, JEOL JXA-8530F analyzer) as shown in Fig.1. The current-voltage (I-V) characteristic of Ti/Au/Cu-electrode on the n-type (111) Si wafer exhibited ohmic behavior. The substrates of single-crystalline n-type Si were commercial products grown by the Czochralski (CZ) process. The electrical resistivity (ρ), Seebeck coefficient (S) and Hall coefficient (R_H) of n-type Si wafer were measured in the temperature range from 80K to 395K using commercial equipment of Toyo Corp, ResiTest8300. The carrier concentration (n) and mobility (μ) were determined using R_H.

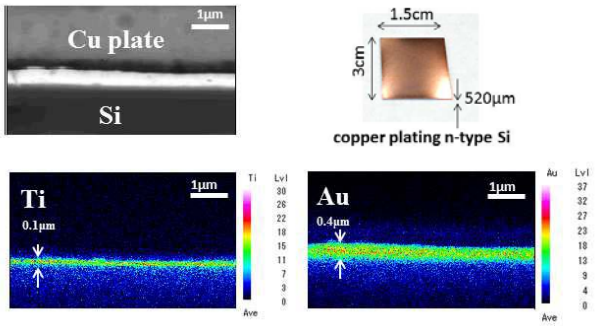

Fig.1 SEM image and EPMA micrographs of n-type Si wafer

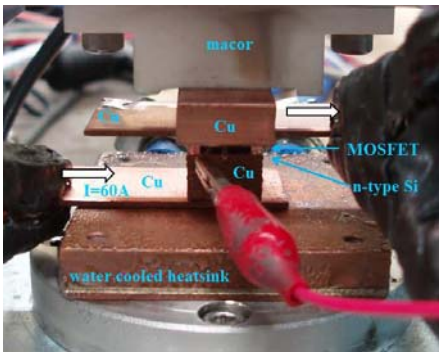

Fig.2 experimental setup to estimate device

The experimental setup used is shown in Fig. 2. The power MOSFET and the n-type Si wafer were located between upper copper block and lower copper block. They were wedged between the macor and the water cooled heatsink by using the screw-type pressing machine. In this system, the electric current of 60A flowed in the self-cooling device from lower to upper direction using the DC power supply (EX-1500L2, TAKASAGO), where the voltage of 10V was applied between the gate and the source in the power MOSFET. The water temperature in the heatsink was maintained 4℃±2℃ constantly by the cooling water circulation system (CA-1112, EYELA). To determine whether the self-cooling device remove the Joule heat from the power MOSFET, we studied the time dependence of the temperature distribution of the self-cooling device. The temperature distribution of the upper side in this system was measured every 10 minutes in an hour using the infrared thermography (TVS-200EX, NEC Avio) and analyzed by the software of InfReC Analyzer (NS9500, NEC Avio).

RESULTS AND DISCUSSION

The electrical resistivity (ρ) for n-type Si wafer was measured from 80K up to 395K by a van der Pauw technique with a current of 10mA. Figure 3(a) shows the electrical resistivity (ρ) as a function of temperature for n-type Si wafer. From this result, the temperature dependence of ρ exhibits a semiconducting behavior below room temperature, while a metallic character above room temperature. In particular, the ρ value at room temperature shows a low value, i.e., ρ=18.8$m\Omega$cm. The Seebeck coefficient (S) for n-type Si wafer was also measured from 80K up to 395K using a temperature difference electromotive force measurement method. As shown in Fig.3(b), the absolute value of S at room temperature shows a large value, i.e., |S|=688μV/K. The power factor ($|S|^2/\rho$) at room temperature is estimated 2.52mW/mK^2. Therefore, the n-type Si wafer is suitable for the thermoelectric material of the self-cooling device because of a high thermal conductivity (κ) of the single crystal Si. The Hall coefficient (R_H) was also measured in order to estimate the carrier concentration ($n=1/eR_H$) and the Hall mobility ($\mu=R_H/\rho$), respectively. In particular, the values of n and μ at room temperature show 1.09×10^{18}cm^{-3} and 300cm^2/Vs, respectively. Results show a very good agreement with the electron drift mobility as a function of donor concentration in n-type Si elucidated by Jacoboni *et al.* [7] as shown in Fig.3(c).

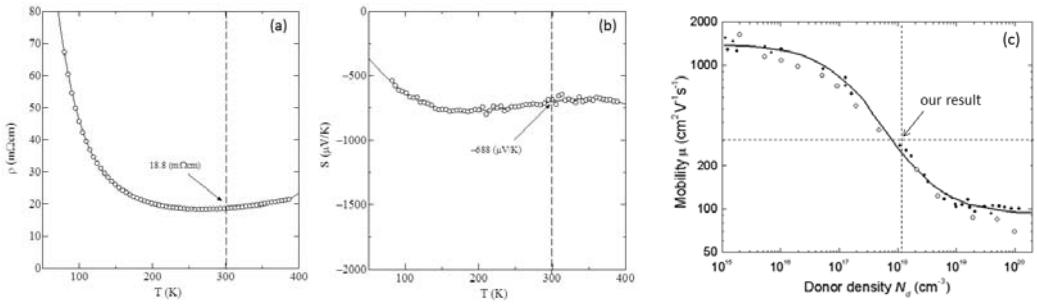

Fig.3 temperature dependence of (a) electrical resistivity and (b) Seebeck coefficient and (c) electron drift mobility as a function of donor concentration in n-type Si elucidated by Jacoboni *et al.* [7]

Figure 4(a) shows the temperature distribution of Joule heat from the power MOSFET filmed by the infrared thermography after 40 minutes. The power MOSFET was located between upper copper block and lower copper block. The electric current of 60A flowed in the system from lower (the drain in the power MOSFET) to upper (the source in the power MOSFET) direction, where the voltage of 10V was applied between the gate and the source in the power MOSFET. The water temperature in the heatsink was maintained 4℃±2℃ constantly by the cooling water circulation system. The Joule heat generated from the power MOSFET is estimated 5 - 6W because of the static drain-to-source on-resistance of $1.5m\Omega$. Figure 4(c) shows the time dependence of the Joule heat (red closed circles) and the input electrical power (red line) and both of them are remain constant for any time. The Joule heat is measured 6.0W from the voltage of 0.10V between the drain and the source in the power MOSFET. It is found that about 10% of the Joule heat includes the heat from the contact resistance. The input electrical power of 48W is estimated from the voltage (0.80V) of the DC power supply. As shown in Fig.4(b), the temperature distribution of the upper side analyzed by the software of InfRec Analyzer NS9500 is in the range 27.2 to 36.0℃. In particular, the temperature distribution shows the peak of the pixel value at 32.9℃. This indicates that the average temperature of the upper side in this system is at 32.9℃ after 40 minutes.

Figure 5(a) shows the temperature distribution of Joule heat from the power MOSFET with the copper plating n-type Si wafer filmed by the infrared thermography after 40 minutes. The copper plating n-type Si wafer was located under the power MOSFET. The electric current of 60A flowed in the system from lower (the drain in the power MOSFET) to upper (the source in the power MOSFET) direction so that the Peltier heat flows in the direction opposite to the current of 60A in the n-type Si wafer. The voltage of 10V was applied between the gate and the source in the power MOSFET and the water temperature in the heatsink was maintained 4℃±2℃ constantly. The Joule heat generated from the power MOSFET with the copper plating n-type Si wafer is estimated 7 - 8W due to an additional Joule heat which includes the heat from the n-type Si wafer itself and the contact resistance. Figure 5(c) shows the time dependence of both the Joule heat and the Peltier heat (blue closed circles) and the input electrical power (blue line), where red closed circles and line are equal to those in Fig.4(c). The voltage between the drain and the source in the power MOSFET is measured about 0.17V for any time. The input electrical power of 52W is estimated from the voltage (0.87V) of the DC power supply, where the increase of the input electrical power between the blue line and the red one is about 4W.

Figure 5(b) shows the temperature distribution of the upper side analyzed by the software of InfRec Analyzer NS9500 is in the range 27.1 to 38.4℃. In particular, the temperature distribution shows the peak of the pixel value at 32.2℃ which is lower than the result showed in Fig.4(b). This indicates that the average temperature of the upper side in this system is cooled down about 0.7℃ after 40 minutes despite enlargement of the temperature distribution range. If it is assumed that the temperature distribution in the range from 36.0 to 38.4℃ is due to a part of the Peltier heat, we can explain the increase of the voltage (about 0.07V) between the drain and the source in the power MOSFET. As shown in Fig.5(c), it is assumed that both the Joule heat of about 8W and the Peltier heat of about 2W generates in the self-cooling device, the heat removal of the upper side in this system can be explained reasonably. If the Joule heat of 10W generates in the self-cooling device, the enhancement of high temperature distribution should occur in the upper side in this system. Therefore, the Peltier heat should make a contribution to cool down the power MOSFET with the copper plating n-type Si wafer. This fact indicates that the copper plating n-type Si wafer is suitable for the thermoelectric materials for use in the self-cooling device which removes the heat generation on the power MOSFET by using the heat flux both by thermal conduction and by Peltier effect.

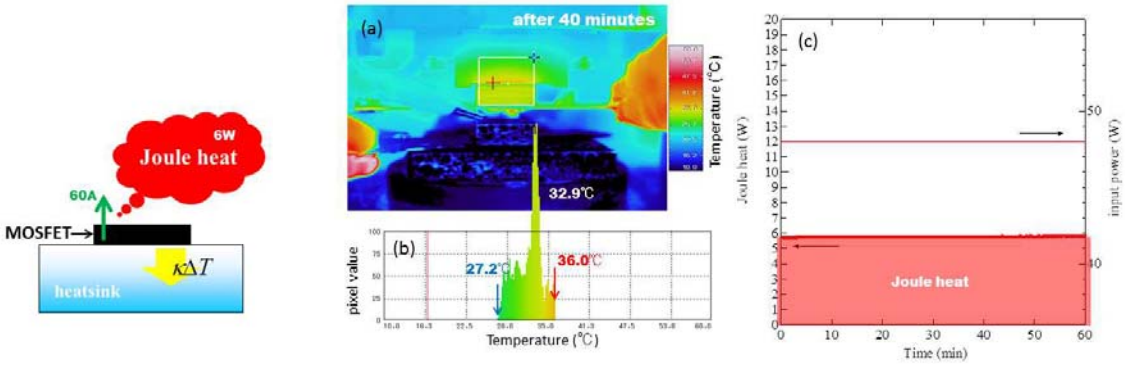

Fig.4 temperature distribution of (a) experimental setup and (b) upper side after 40 minutes, and (c) time dependence of heat and input power, where κ⊿T represents the heat flux by the thermal conduction

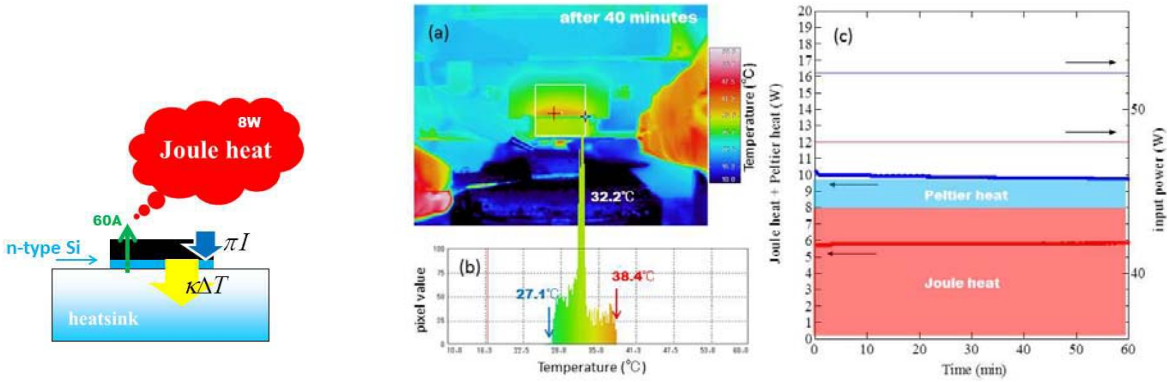

Fig.5 temperature distribution of (a) experimental setup and (b) upper side after 40 minutes, and (c) time dependence of heat and input power, where πI represents the heat flux by the Peltier effect

CONCLUSION

In order to improve heat removal or cooling for the power MOSFET, we developed the self-cooling device which consists of the power MOSFET and the n-type Si wafer and estimated the heat flux both by the thermal conduction and by the Peltier effect using the measurement of the time dependence of the temperature distribution. We revealed that the average temperature of the upper side of the power MOSFET was cooled down by the addition of the copper plating n-type Si wafer. We conclude, as a result of this study, that the n-type Si wafer is one of the candidate materials for use in self-cooling devices.

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