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Electric Current Dependence of a Self-Cooling Device Consisting of Silicon Wafers Connected to a Power MOSFET

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A self-cooling device has been developed by combining a commercial *n*-channel power metal–oxide–semiconductor field-effect transistor (MOSFET) and single-crystalline Sb-doped *n*-type or B-doped *p*-type silicon wafers in order to improve the heat removal or cooling quantitatively. The electric current dependence of the temperature distribution in the self-cooling device and the voltage between the source and drain electrodes have been measured to estimate the Peltier heat flux. We found that the average temperature is decreased for a power MOSFET in which an electric current of 50 A flows. In particular, the average temperature of the power MOSFET was decreased by 2.7°C with the *n*-type Si wafer and by 3.5°C with the *p*-type Si wafer, although an electric current of 40 A makes little difference. This certainly warrants further work with improved measurement conditions. Nonetheless, the results strongly indicate that such *n*-type or *p*-type silicon wafers are candidate materials for use in self-cooling devices.

Key words: Self-cooling device, power MOSFET, silicon wafer, thermal conduction, Joule heat, Peltier heat, infrared thermography

INTRODUCTION

Silicon semiconductor power devices, including metal–oxide–semiconductor field-effect transistors (MOSFETs), insulated gate bipolar transistors (IGBTs), and central processing units (CPUs), are used in daily life to enable our modern lifestyles. During use of electrical equipment incorporating such devices, improvement of heat removal or cooling is one of the most important issues, because they do not function correctly if operated at temperatures above 150°C. There are two conventional ways to remove heat from power devices. One is to use a fin and fan connected to the power devices, i.e., a conventional cooling system based only on thermal conduction. The other is to use a Peltier module with a large fin and fan using only the Peltier heat flux. However, when using these methods to cool power devices, the electric power consumption is increased because the Peltier module, fan, and power devices need different direct-current (DC) power supplies for their operation. This is one of the reasons why Peltier modules are not applied for cooling power devices.

In recent studies, a self-cooling device[1–4] has been proposed and investigated for new cooling schemes to remove heat from power devices. This device consists of *n*-type or *p*-type thermoelectric material connected to the power device. Figure 1 shows a schematic of the structure of such a self-cooling device. As the electric current flows from the bottom (or top) to the top (or bottom), heat is transferred by the Peltier flux and thermal conduction from the hot side ($T = T_H$) to the cold side ($T = T_L$), where the endothermic part is formed of the *p*-type (or *n*-type) thermoelectric material. In this scheme, the thermoelectric materials used in the self-cooling device must have high Seebeck coefficient (S), high electrical conductivity (σ), and high thermal conductivity (κ). Conventional thermoelectric studies usually try to identify materials with low thermal conductivity

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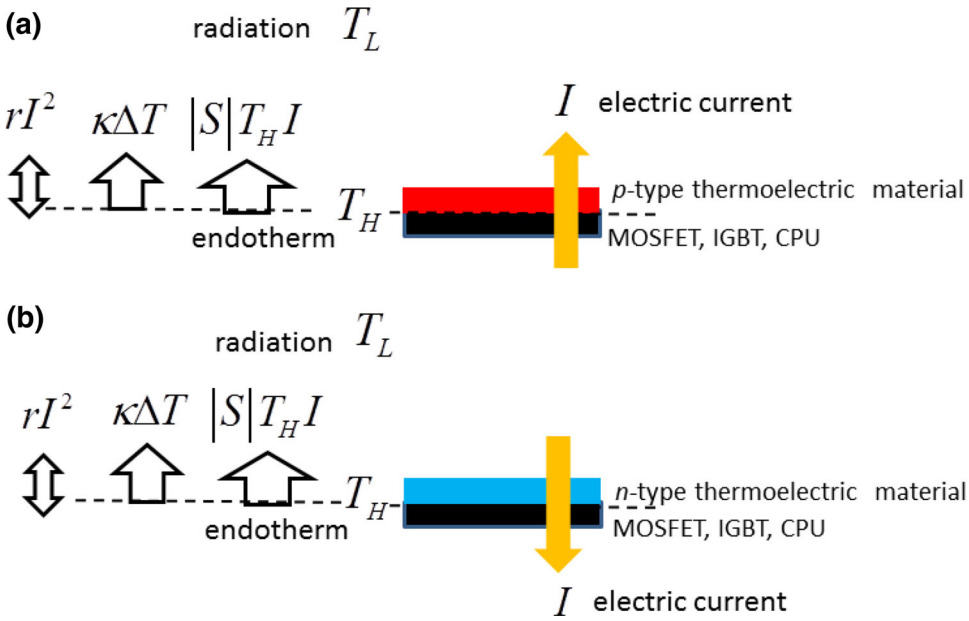

Fig. 1. Schematic structure of the self-cooling device and heat flow in (a) *p*-type or (b) *n*-type thermoelectric materials when an electric current flows, where T_H and T_L are the temperatures of the hot and cold side, respectively.

to use as thermoelectric materials, and many materials with high Seebeck coefficient or high electrical conductivity have been abandoned because of their high thermal conductivity. Fortunately, it is easy to find materials with the combination of high electrical conductivity, high Seebeck coefficient, and high thermal conductivity for use in self-cooling devices, because materials with higher thermal conductivity usually also have higher electrical conductivity. Typical materials with high thermal conductivity include, for example, silicon carbide (κ = 490 W/m K) and silicon (κ = 150 W/m K).

Nakatsugawa et al.[3] investigated the thermoelectric properties of polycrystalline SiC/Si composites, and improved the performance of the self-cooling device. Fukuda et al.[4] optimized the carrier concentration in single-crystalline SiC and dense sintered polycrystalline SiC and found that 4H-SiC with a high carrier density yielded good performance of the self-cooling device. Single-crystalline Si is also expected to show higher performance than 4H-SiC because of its higher power factor.[5–8] The large values of the Seebeck coefficient of single-crystal Si have been studied in detail.[5] In particular, recent study suggested that the Seebeck coefficient of heavily doped Si exhibits a hump at a carrier concentration on the order of 10^{19} cm^{-3}, while the electrical resistivity decreases linearly with increasing carrier concentration.[8] Thus, single-crystalline silicon may be one of the candidate materials for use in self-cooling devices.

We have investigated the self-cooling device using an Sb-doped *n*-type Si wafer and reported the heat removal from a power MOSFET qualitatively.[9] Fukuda et al.[10] suggested that a self-cooling device based on a B-doped *p*-type Si wafer with high carrier density could exhibit good heat removal performance. However, quantitative understanding of single-crystalline *n*-type or *p*-type silicon for use in the self-cooling device is still lacking. The aim of this study is to develop the self-cooling device using an *n*-type or *p*-type silicon wafer to estimate the heat removal quantitatively in order to improve the cooling of power MOSFETs.

EXPERIMENTAL PROCEDURES

The self-cooling device consisted of a commercial *n*-channel power MOSFET (IRF1324PbF, static drain-to-source on-resistance of 1.5 mΩ; International IOR Rectifier) on a substrate of single-crystalline Sb-doped *n*-type or B-doped *p*-type silicon with (111) orientation which was cut into rectangular specimens with dimensions of 30 mm × 30 mm and thickness of 520 μm. The single-crystalline silicon substrates were commercial products grown by the Czochralski (CZ) process, being low-resistivity specimens. The surfaces of the Si wafer were coated with 0.1 μm of titanium to ensure adhesion and 0.4 μm of gold deposited by sputtering. Then, copper electrodes were fabricated on both surfaces with thickness of about 2 μm, deposited by copper plating. The chemical composition of the coatings was clearly verified by field-emission electron probe x-ray microanalysis (EPMA, JXA-8530F analyzer; JEOL). In addition, the current–voltage (I–V) characteristic of the Ti/Au/Cu electrode on the *n*-type or *p*-type silicon wafer did not exhibit a Schottky barrier. The electrical resistivity (ρ), Seebeck coefficient (S), and

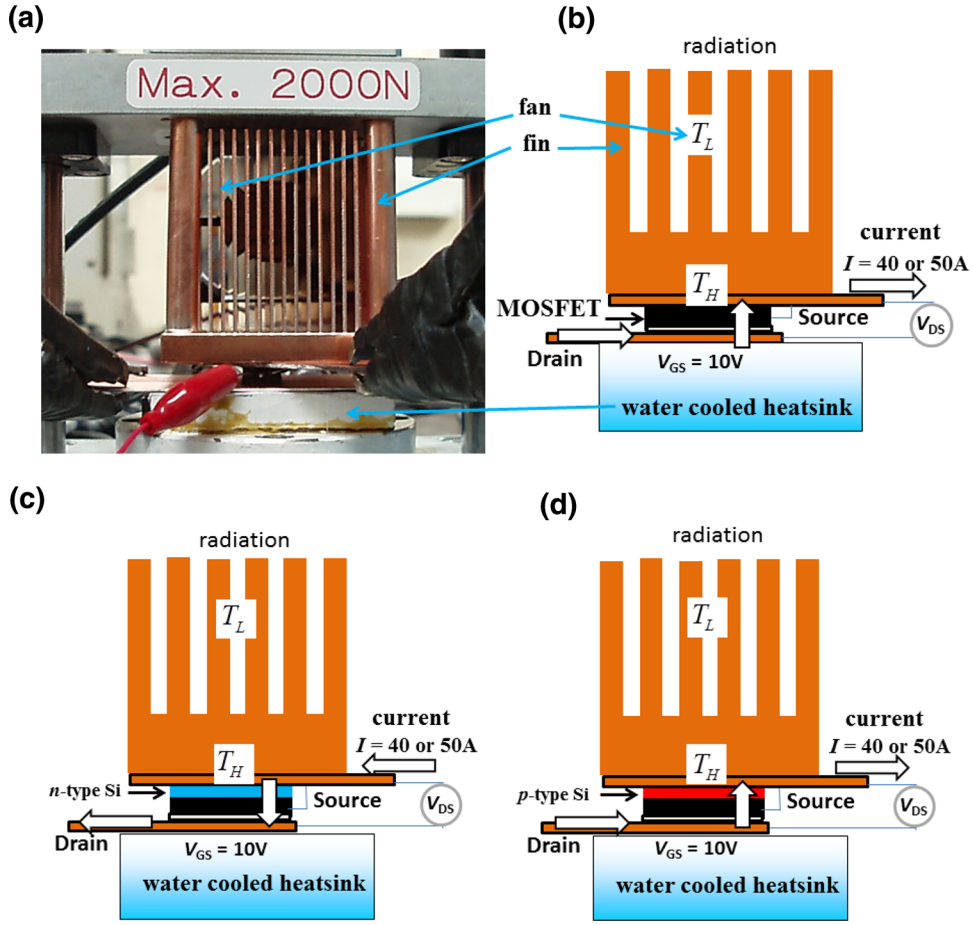

Fig. 2. (a) Experimental setup used to investigate the self-cooling device, and schematic illustrations of (b) the MOSFET only, (c) the MOSFET with the *n*-type Si wafer, and (d) the MOSFET with the *p*-type Si wafer, where T_L is the temperature of the upper side consisting of the fin cooled by the fan.

Hall coefficient (R_H) of the Si wafers were measured in the temperature range from −193°C to 122°C using commercial equipment from Toyo Corp (Resi-Test8300).

Figure 2 shows the experimental setup used to investigate the self-cooling device (a) and schematic illustrations of the MOSFET only (b), the MOSFET with the *n*-type Si wafer (c), and the MOSFET with the *p*-type Si wafer (d), fixed between the fin and a water-cooled heat sink. The white arrow indicates the direction of electric current (I = 40 A or 50 A) flow when a voltage of 10 V is applied between the gate and source of the power MOSFET. The power MOSFET and the *n*-type or *p*-type Si wafer were fixed between a fin and a water-cooled heat sink using a screw-type pressure device, where the fin was cooled by a fan throughout the measurements. The water temperature in the heat sink was maintained constantly at about 3°C using a cooling water circulation system (CA-1112; EYELA). In this system, the electric current is flowed along the direction indicated by the white arrow by a DC power supply (EX-1500L2; TAKASAGO), so that both the Peltier heat flux and thermal conduction can be transferred from the power MOSFET to the upper side consisting of the fin cooled by the fan. Of course, the thermal conduction is also transferred from the power MOSFET to the lower side consisting of the water-cooled heat sink. To determine whether the self-cooling device can remove the Joule heat from the power MOSFET, we measured the time dependence of the temperature distribution of the self-cooling device using infrared thermography (TVS-200EX; NEC Avio) and analyzed the temperature distribution along a line profile using an InfReC analyzer (NS9500; NEC Avio) every 10 min for 1 h. The voltage between the source and drain electrodes, V_{DS}, was also measured to estimate the Joule heat and the Peltier heat from the *n*-type or *p*-type silicon wafer.

RESULTS AND DISCUSSION

The electrical resistivity (ρ) and Hall coefficient (R_H) of the silicon wafer with Ti/Au deposited by sputtering were measured from −193°C to 122°C using the van der Pauw technique for current of 10 mA and 100 mA. Figure 3a shows the electrical resistivity as a function

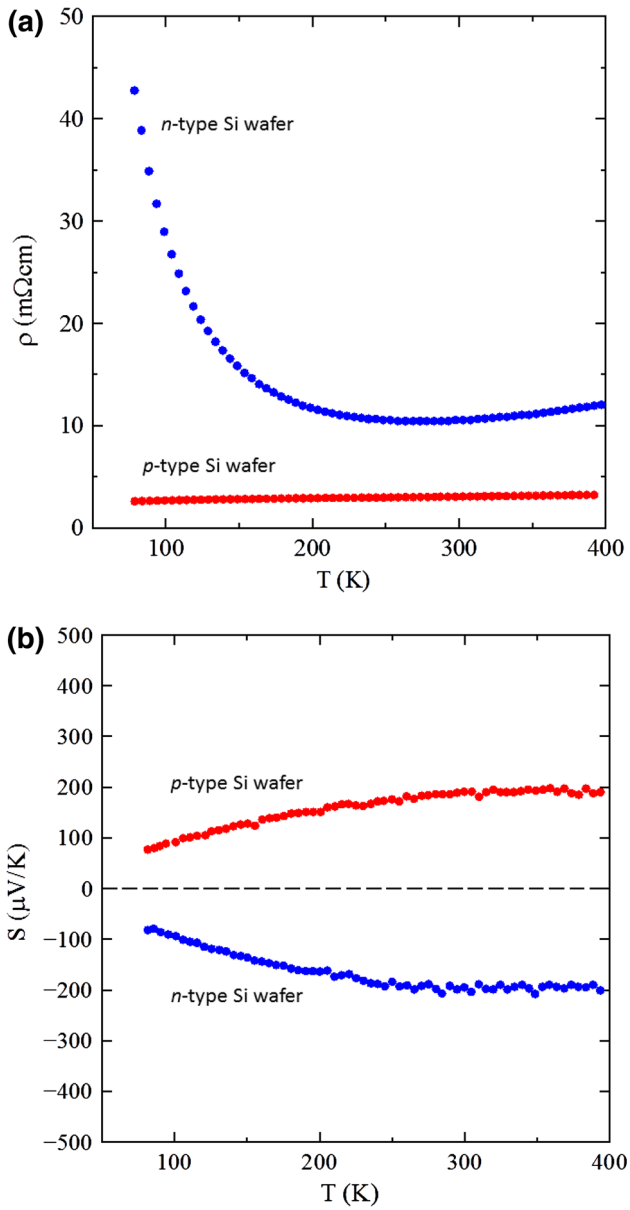

Fig. 3. Temperature dependence of (a) the electrical resistivity (ρ) and (b) the Seebeck coefficient (S) for the n-type and p-type silicon wafers.

of temperature for the n-type and p-type silicon wafers. In particular, the resistivity at room temperature shows a low value, i.e., ρ = 10.3 mΩ cm for the n-type Si wafer and ρ = 3.00 mΩ cm for the p-type Si wafer. Thus, the resistance of the n-type and p-type Si wafers cut into square specimens with dimensions of 30 mm × 30 mm and thickness of 520 μm is estimated to be 0.060 mΩ and 0.017 mΩ, respectively. The Seebeck coefficient (S) for a silicon wafer with Ti/Au deposited by sputtering was also measured from −193°C up to 122°C by measuring the electromotive force under a temperature difference. As plotted in Fig. 3b, the absolute value of S at room temperature was $|S|$ = 200 μV/K for the n-type Si wafer and $|S|$ = 193 μV/K for the p-type Si wafer. This means that the power factor at room temperature is 0.4×10^{-3} W/m K^2 for the n-type Si wafer and 1.2×10^{-3} W/m K^2 for the p-type Si wafer. At room temperature, the carrier concentration ($n = 1/e|R_H|$) was 5×10^{18} cm^{-3} for the n-type Si wafer and 9×10^{19} cm^{-3} for the p-type Si wafer. In previous studies, the Seebeck coefficient of the silicon wafer was sensitive to the carrier density.[5–8] Fukuda et al.[10] suggested that a p-type Si wafer with carrier density of 1.6×10^{19} cm^{-3} has a power factor of 4.8×10^{-3} W/m K^2. Our samples show similar dependences.

Figure 4a shows the temperature distribution of the Joule heat from the MOSFET recorded by infrared thermography after 60 min. The power MOSFET was fixed between the fin and the water-cooled heat sink. An electric current of 40 A flowed in the system from below (the drain electrode in the power MOSFET) to above (the source electrode in the power MOSFET), when a voltage of 10 V was applied between the gate and source of the power MOSFET. The Joule heat generated by the power MOSFET is estimated at 2.40 W based on the static drain-to-source on-resistance of 1.5 mΩ. In fact, the voltage between the drain and source electrodes of the power MOSFET, V_{DS} = 60 mV, remains constant for any time. After 60 min, the temperatures on the upper side of the power MOSFET, on the power MOSFET, and on the lower side of the power MOSFET were 23.2°C, 12.3°C, and 7.3°C, respectively. The time dependence of the temperatures is presented in Fig. 4b. In particular, the average temperatures on the upper side of the power MOSFET, on the power MOSFET, and on the lower side of the power MOSFET were 23.3(2)°C, 12.6(4)°C, and 7.4(2)°C, respectively, where the number in parenthesis indicates the standard deviation.

As shown in Fig. 5a, the power MOSFET with the n-type silicon wafer was fixed between the fin and the water-cooled heat sink, and the temperature distribution due to the Joule heat was recorded by infrared thermography after 60 min. An electric current of 40 A flowed in the self-cooling device from above to below, so that the Peltier heat was absorbed from the lower side of the power MOSFET to the upper side, i.e., the fin or surroundings. The Joule heat generated by the power MOSFET with the n-type Si wafer was estimated as about 2.50 W, where the Joule heat of the n-type Si wafer is 95 mW for an electric current of 40 A. The voltage between the drain and source electrodes in the power MOSFET (V_{DS} = 129 mV) remains constant, so that the Peltier heat from the n-type Si wafer is estimated as $|S|TI$ = 2.66 W, where $|S|T$ = 66.5 mV (corresponding to $|S|$ = 222 μV/K, T = 27°C) is the Peltier coefficient. After 60 min, the temperatures on the upper side of the power MOSFET, on the power MOSFET, and on the lower side of the power MOSFET were 25.0°C, 11.4°C, and 7.3°C, respectively. As shown in Fig. 5b, the average temperatures on the upper side of the power MOSFET, on the power MOSFET, and on the lower side of the power MOSFET were 24.3(3)°C,

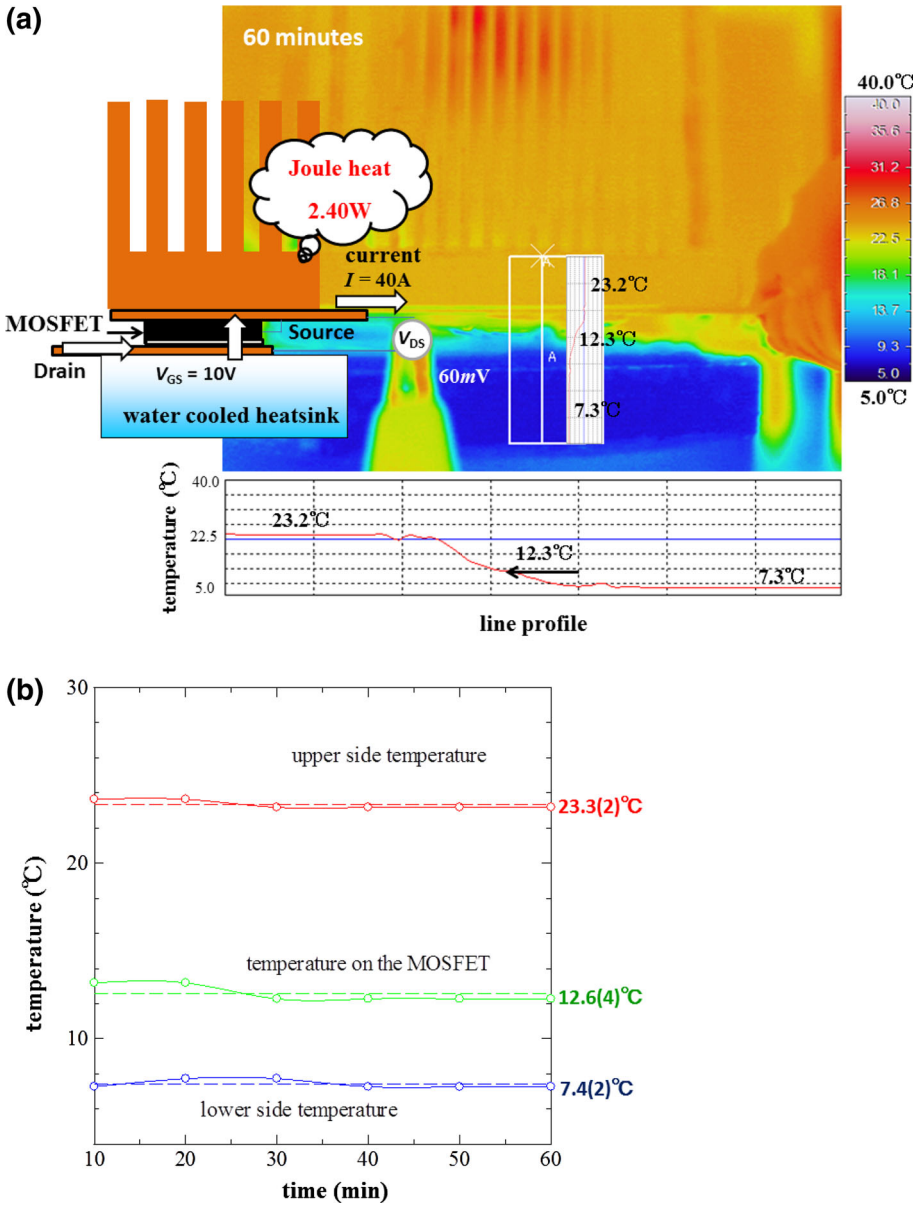

Fig. 4. (a) Schematic illustration and temperature distribution of the power MOSFET recorded by infrared thermography after 60 min when an electric current of 40 A flows. (b) Time dependence of the temperatures on the upper side of the power MOSFET (red open circle), on the power MOSFET (green open circle), and on the lower side of the power MOSFET (blue open circle) (Color figure online).

12.1(7)°C, and 7.3(0)°C, respectively, as indicated by open circles in Fig. 4b. The average temperature on the MOSFET does not change; however, that of the upper side increases after installation of the *n*-type Si wafer. Though heat removal from the MOSFET could not be observed, the data indicate that heat radiation increases with increasing Peltier heat flux from the *n*-type Si wafer.

The power MOSFET with the *p*-type silicon wafer was then fixed between the fin and the water-cooled heat sink. The temperature distribution of the Joule heat was recorded by infrared thermography after 60 min, as shown in Fig. 6a. An electric current of 40 A flowed in the self-cooling device from below to above, so that the Peltier heat was absorbed from the lower side to the fin or surroundings. The Joule heat generated by the power MOSFET with the *p*-type Si wafer was estimated as about 2.43 W, where the Joule heat of the *p*-type Si wafer is 27 mW for an electric current of 40 A. The voltage between the drain and source electrodes in the power MOSFET (V_{DS} = 132 mV) remains constant, so that the Peltier heat from the *p*-type Si wafer is estimated as $|S|TI$ = 2.85 W, where $|S|T$ = 71.3 mV (corresponding to $|S|$ = 238 μV/K, T = 27°C) is the Peltier coefficient. After 60 min, the temperatures on the

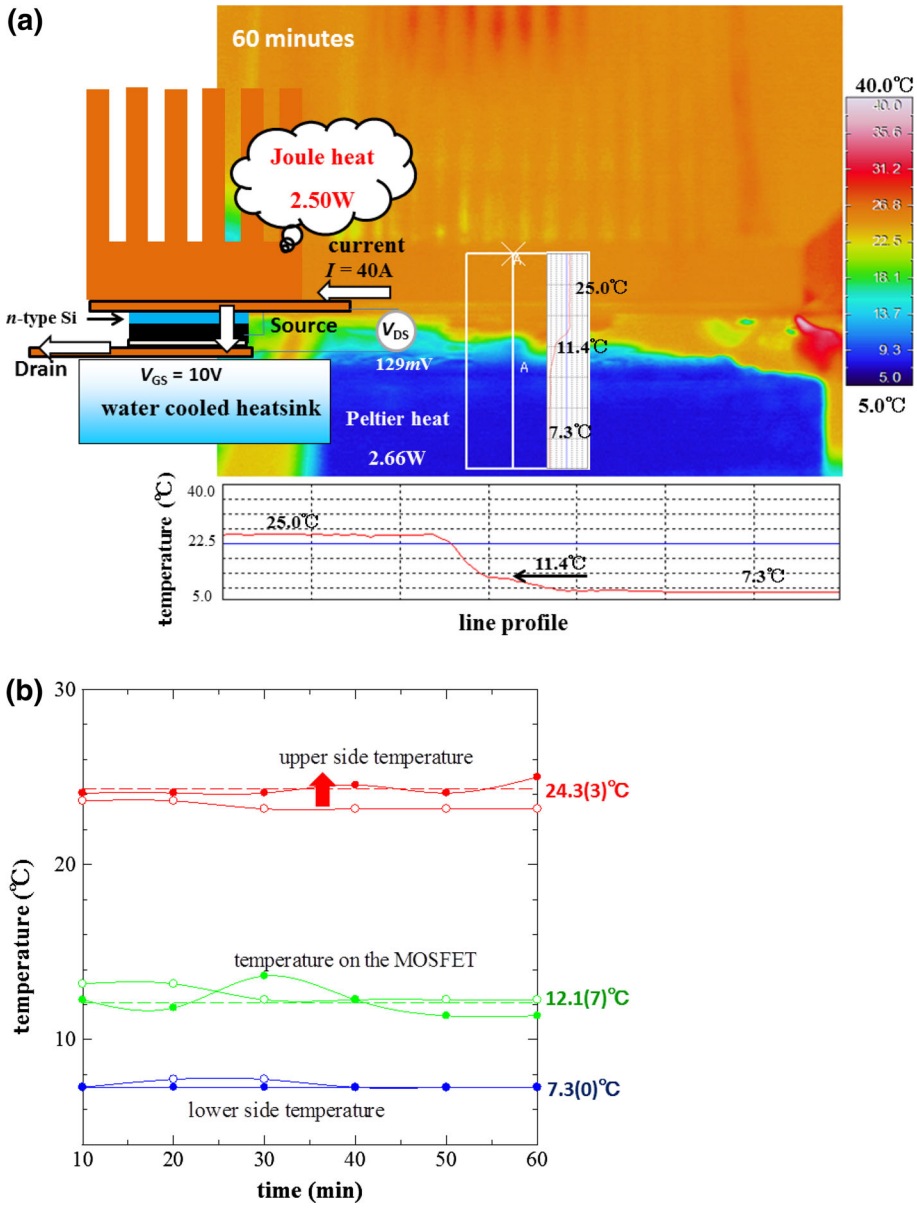

Fig. 5. (a) Schematic illustration and temperature distribution of the power MOSFET with the *n*-type Si wafer recorded by infrared thermography after 60 min when an electric current of 40 A flows. (b) Time dependence of the temperatures on the upper side of the power MOSFET with the *n*-type Si wafer (red closed circle), on the power MOSFET with the *n*-type Si wafer (green closed circle), and on the lower side of the power MOSFET with the *n*-type Si wafer (blue closed circle) (Color figure online).

upper side of the power MOSFET, on the power MOSFET, and on the lower side of the power MOSFET were 25.0°C, 12.3°C, and 7.3°C, respectively. As shown in Fig. 6b, the average temperatures on the upper side of the power MOSFET, on the power MOSFET, and on the lower side of the power MOSFET were 24.9(1)°C, 12.1(3)°C, and 7.3(3)°C, respectively, as indicated by open circles in Fig. 4b. The average temperature on the MOSFET does not change; however, that of the upper side increases by 1.6°C. This indicates that heat radiation from the self-cooling device increases with increasing Peltier heat flux from the *p*-type Si wafer.

Figure 7a shows the temperature distribution of the Joule heat from the MOSFET recorded by infrared thermography after 60 min. An electric current of 50 A flowed in the system from below (the drain electrode in the power MOSFET) to above (the source electrode in the power MOSFET). The Joule heat generated by the power MOSFET is estimated as 3.85 W. The voltage between the drain and source electrodes in the power MOSFET, V_{DS} = 77 mV, remains constant for any time. After 60 min, the temperatures on the upper side of the power MOSFET, on the power MOSFET, and on the lower side of the power MOSFET were 24.1°C, 15.5°C, and 7.7°C,

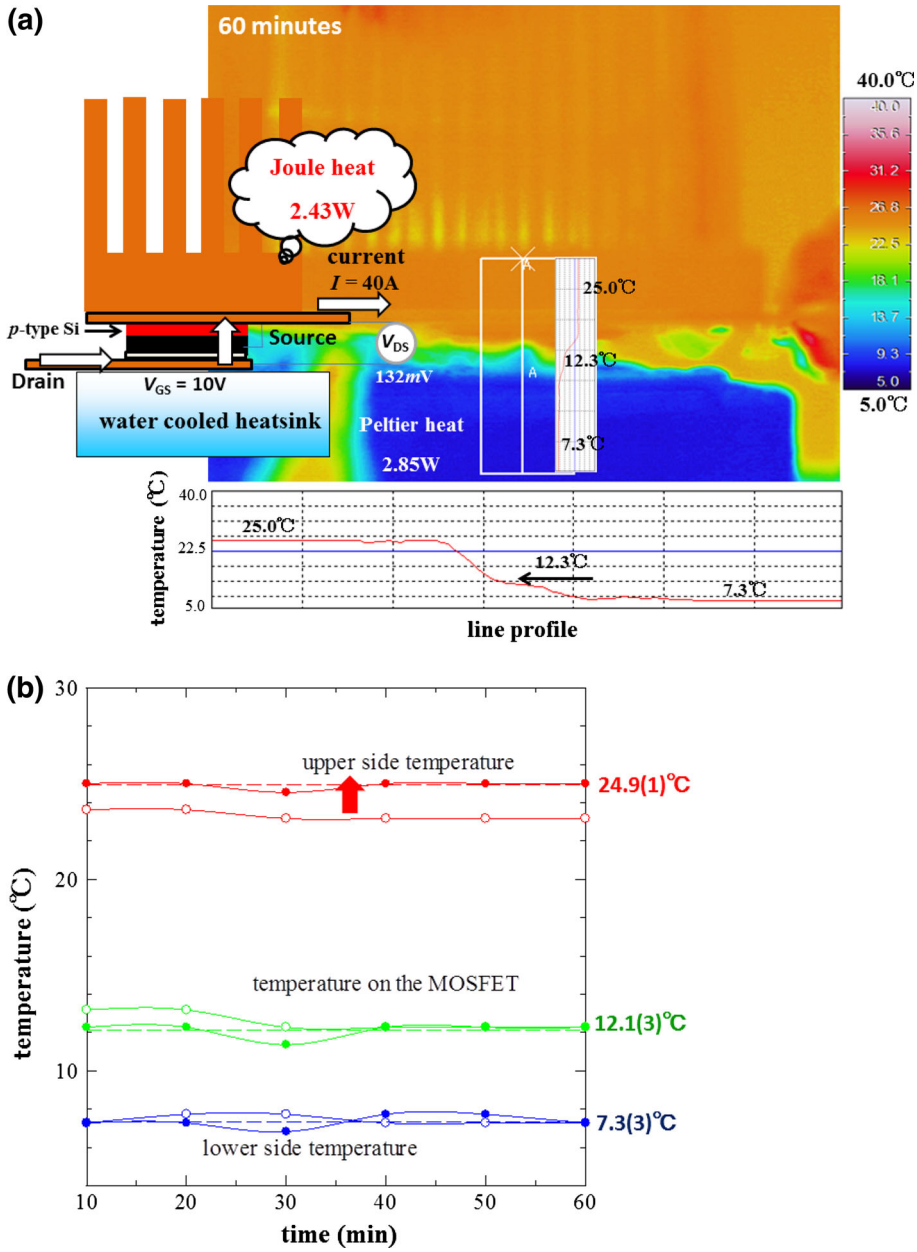

Fig. 6. (a) Schematic illustration and temperature distribution of the power MOSFET with the *p*-type Si wafer recorded by infrared thermography after 60 min when an electric current of 40 A flows. (b) Time dependence of the temperatures on the upper side of the power MOSFET with the *p*-type Si wafer (red closed circle), on the power MOSFET with the *p*-type Si wafer (green closed circle), and on the lower side of the power MOSFET with the *p*-type Si wafer (blue closed circle) (Color figure online).

respectively. In particular, the temperature on the power MOSFET increases rapidly with increasing electric current. This indicates that the Joule heat from the power MOSFET is larger than for an electrical current of 40 A. As shown in Fig. 7b, the average temperatures on the upper side of the power MOSFET, on the power MOSFET, and on the lower side of the power MOSFET were 24.4(4)°C, 15.9(5)°C, and 7.9(5)°C, respectively.

Figure 8a shows the temperature distribution of the Joule heat in the power MOSFET with the *n*-type silicon wafer as recorded by infrared thermography after 60 min. An electric current of 50 A flowed in the self-cooling device from above to below, so that the Peltier heat was absorbed from the lower side of the power MOSFET to the fin or surroundings. The Joule heat was estimated as about 4.00 W, where the Joule heat of the *n*-type Si wafer is 150 mW for an electric current of 50 A. The voltage between the drain and source electrodes in the power MOSFET (V_{DS} = 159 mV) remains constant, so that the Peltier heat from the *n*-type Si wafer is

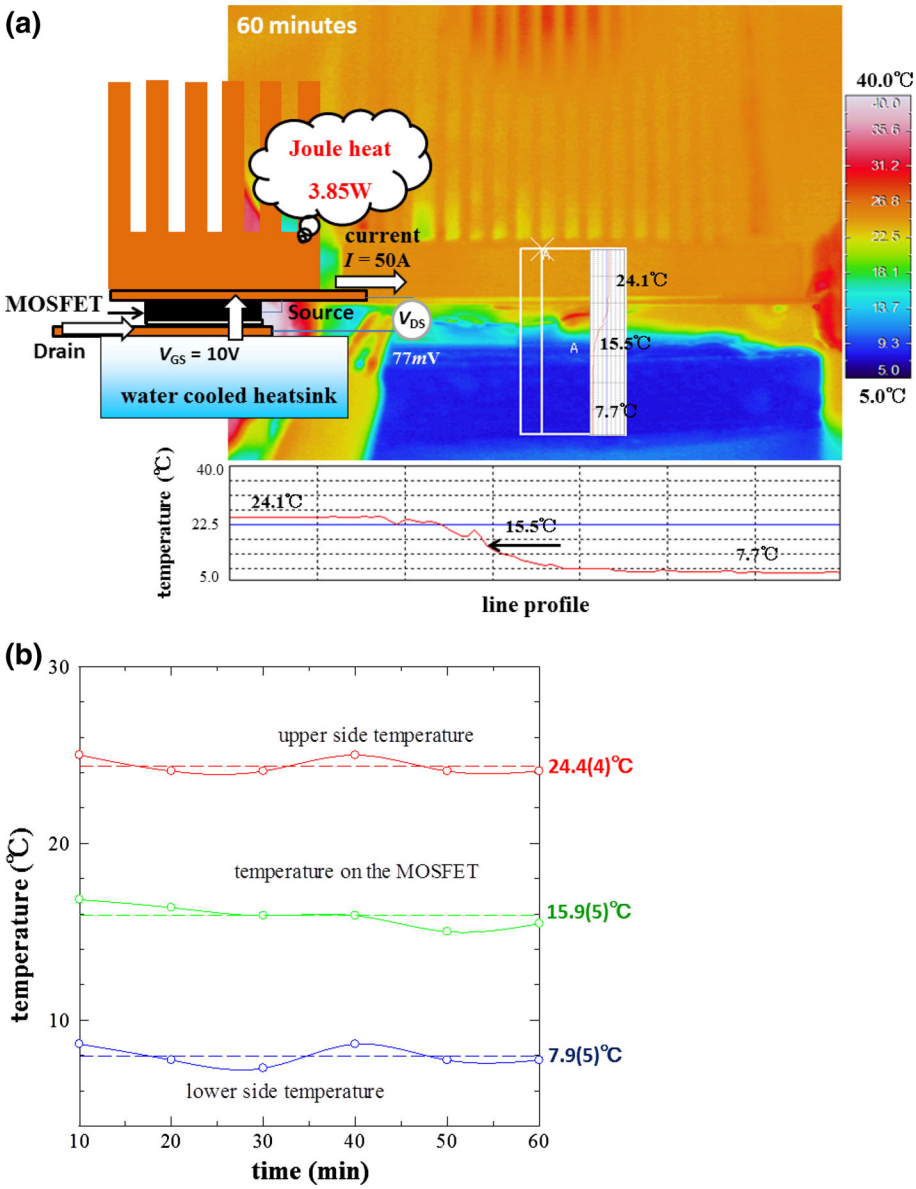

Fig. 7. (a) Schematic illustration and temperature distribution of the power MOSFET recorded by infrared thermography after 60 min when an electric current of 50 A flows. (b) Time dependence of the temperatures on the upper side of the power MOSFET (red open circle), on the power MOSFET (green open circle), and on the lower side of the power MOSFET (blue open circle) (Color figure online).

estimated as $|S|TI$ = 3.95 W, where the Peltier coefficient is $|S|T$ = 79.0 mV. After 60 min, the temperatures on the upper side of the power MOSFET, on the power MOSFET, and on the lower side of the power MOSFET were 25.9°C, 12.7°C, and 7.3°C, respectively. As shown in Fig. 8b, the average temperatures on the upper side of the power MOSFET, on the power MOSFET, and on the lower side of the power MOSFET were 26.1(3)°C, 13.2(4)°C, and 7.5(3)°C, respectively, as indicated by open circles in Fig. 7b. The average temperature of the water-cooled heat sink remained constant throughout the measurements. In contrast, the average temperature of the upper side increased, and that on the power MOSFET was decreased due to the self-cooling device. In particular, the average temperature on the power MOSFET was decreased by 2.7°C with the *n*-type Si wafer. This indicates that the *n*-type silicon wafer is one of the candidate materials for use in self-cooling devices to remove heat from power MOSFETs by both thermal conduction and Peltier heat flux.

Figure 9a shows the temperature distribution of the Joule heat in the power MOSFET with the *p*-type silicon wafer as recorded by infrared thermography after 60 min. An electric current of 50 A flowed in the self-cooling device from below to above, so that the Peltier heat was absorbed from the lower side to the fin or

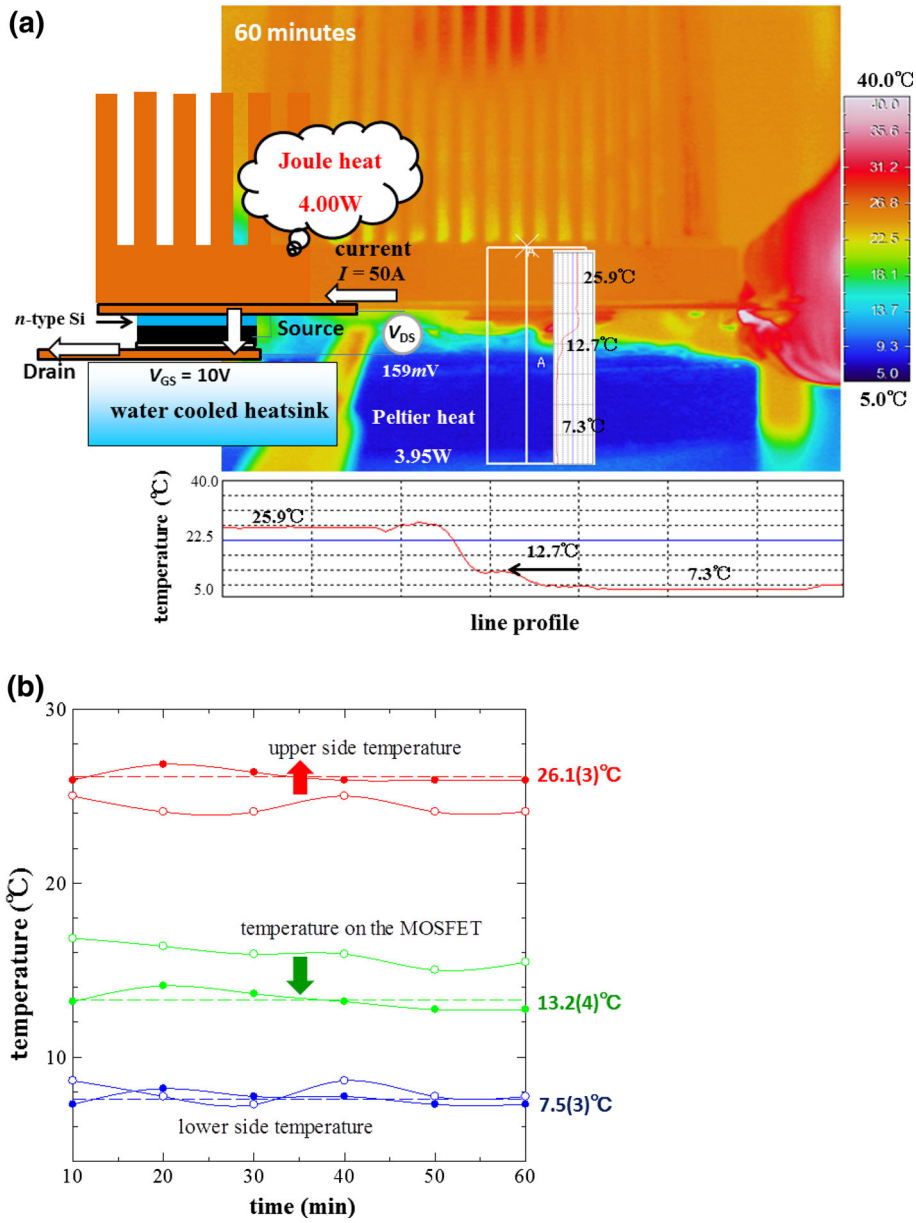

Fig. 8. (a) Schematic illustration and temperature distribution of the power MOSFET with the *n*-type Si wafer recorded by infrared thermography after 60 min when an electric current of 50 A flows. (b) Time dependence of the temperatures on the upper side of the power MOSFET with the *n*-type Si wafer (red closed circle), on the power MOSFET with the *n*-type Si wafer (green closed circle), and on the lower side of the power MOSFET with the *n*-type Si wafer (blue closed circle) (Color figure online).

surroundings. The Joule heat generated by the power MOSFET with the *p*-type Si wafer is estimated as about 3.89 W, where the Joule heat of the *p*-type Si wafer is 43 mW for an electric current of 50 A. The voltage between the drain and source electrodes in the power MOSFET (V_{DS} = 168 mV) remains constant, so that the Peltier heat from the *p*-type Si wafer is estimated as $|S|TI$ = 4.51 W, where the Peltier coefficient is $|S|T$ = 90.2 mV. After 60 min, the temperatures on the upper side of the power MOSFET, on the power MOSFET, and on the lower side of the power MOSFET were 26.4°C, 12.3°C, and 7.7°C, respectively. As shown in Fig. 9b, the average temperatures on the upper side of the power MOSFET, on the power MOSFET, and on the lower side of the power MOSFET were 26.4(3)°C, 12.4(3)°C, and 7.5(2)°C, respectively, as indicated by open circles in Fig. 7b. The average temperature on the upper side increased whereas that on the power MOSFET decreased when applying the self-cooling device. In particular, the average temperature on the power MOSFET was decreased by 3.5°C with the *p*-type Si wafer. This indicates that the *p*-type silicon wafer is also one of the candidate materials for use in the self-cooling device.

Table I presents the average temperatures on the upper side, on the power MOSFET, and on the lower

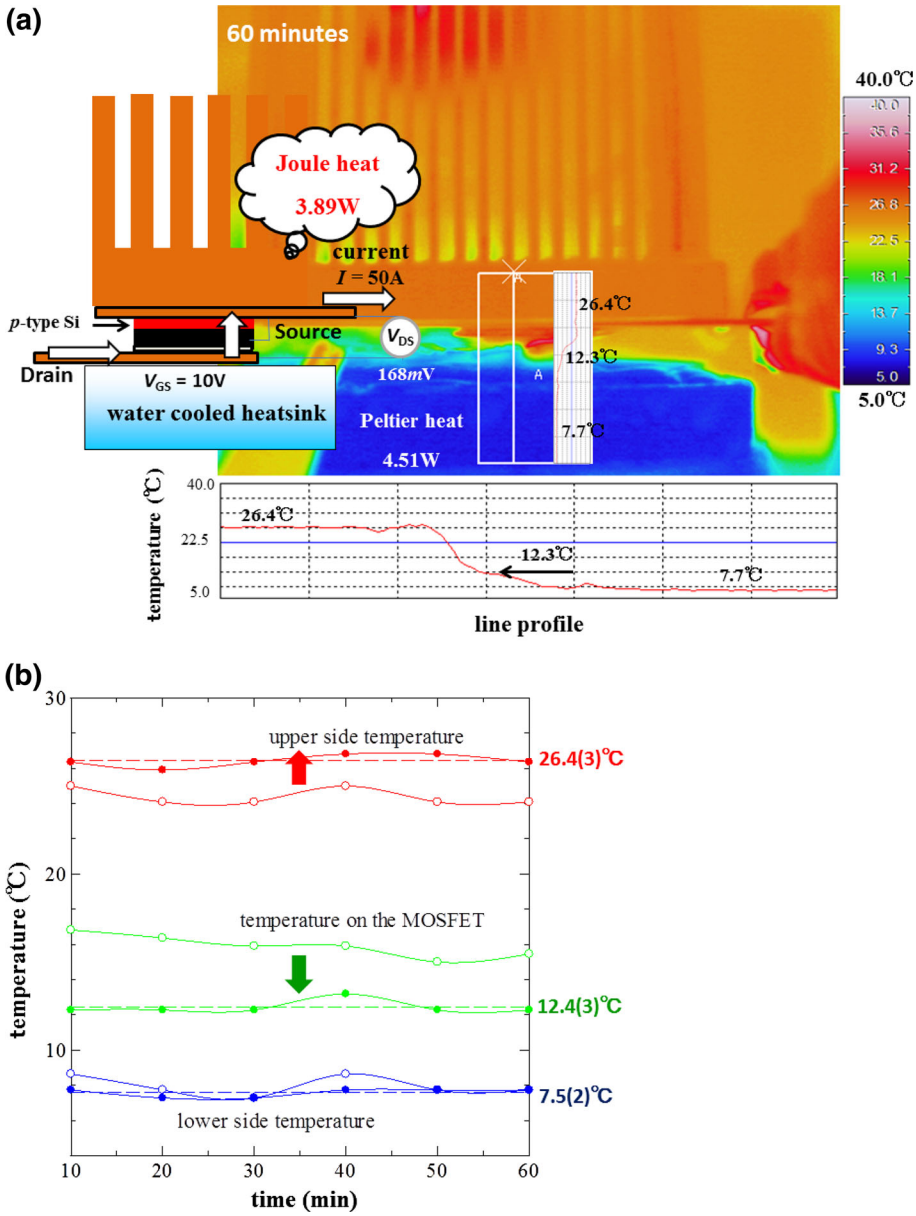

Fig. 9. (a) Schematic illustration and temperature distribution of the power MOSFET with the *p*-type Si wafer recorded by infrared thermography after 60 min when an electric current of 50 A flows. (b) Time dependence of the temperatures on the upper side of the power MOSFET with the *p*-type Si wafer (red closed circle), on the power MOSFET with the *p*-type Si wafer (green closed circle), and on the lower side of the power MOSFET with the *p*-type Si wafer (blue closed circle) (Color figure online).

side, the voltage between the drain and source electrodes connected to the power MOSFET, the Joule heat from the power MOSFET and the silicon wafer, and the Peltier heat from the silicon wafer. The results for the average temperature on the lower side suggest that the water temperature in the heat sink remains constant throughout the measurements. The average temperature on the upper side is increased because of the exhaust heat from the silicon wafer; in contrast, that of the MOSFET is decreased due to the self-cooling device. In particular, the heat removal increases on increasing the electric current from 40 A to 50 A. This indicates that the silicon wafers are candidate materials for use in the self-cooling device by using both thermal conduction and the Peltier heat flux.

CONCLUSIONS

To improve heat removal or cooling for power MOSFETs, we have developed a self-cooling device consisting of an *n*-channel power MOSFET and an *n*-type or *p*-type silicon wafer. The results of this study indicate that the average temperature on the

Table I. Average temperatures of the upper side, the power MOSFET, and the lower side, the voltage between the drain and source electrodes connected to the power MOSFET, the Joule heat from the power MOSFET and the silicon wafer, and the Peltier heat from the silicon wafer

	Current (A)	MOSFET	MOSFET + *n*-Si	MOSFET + *p*-Si
Average temperature of upper side (°C)	40	23.3(2)	24.3(3)	24.9(1)
	50	24.4(4)	26.1(3)	26.4(3)
Average temperature of the MOSFET (°C)	40	12.6(4)	12.1(7)	12.1(3)
	50	15.9(5)	13.2(4)	12.4(3)
Average temperature of lower side (°C)	40	7.4(2)	7.3(0)	7.3(3)
	50	7.9(5)	7.5(3)	7.5(2)
Voltage between drain and source (mV)	40	60	129	132
	50	77	159	168
Joule heat (W)	40	2.40	2.50	2.43
	50	3.85	4.00	3.89
Peltier heat (W)	40	–	2.66	2.85
	50	–	3.95	4.51

upper side of the power MOSFET with the *n*-type or *p*-type silicon wafer is increased because of heat radiation. The average temperature of the water-cooled heat sink remains constant throughout the measurements. In contrast, the average temperature on the power MOSFET is decreased, when an electric current of 50 A flows. In particular, the average temperature on the power MOSFET was decreased by 2.7°C with the *n*-type Si wafer and by 3.5°C with the *p*-type Si wafer, although an electric current of 40 A makes little difference. This strongly indicates the electric current dependence of the self-cooling device. Therefore, the *n*-type and *p*-type silicon wafers are candidate materials for use in the self-cooling device.

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