

Self-cooling on power MOSFET using n-type Si wafer

H.Nakatsugawa^{1*}, T.Sato¹, Y.Okamoto², T.Kawahara³, and S.Yamaguchi³

¹ Yokohama National University, 79-5 Tokiwadai, Hodogaya, Yokohama, Kanagawa, Japan

² National Defense Academy, 1-10-20 Hashirimizu, Yokosuka, Kanagawa, Japan

³ Chubu University, 1200 Matsumoto-cho, Kasugai, Aichi, Japan

*E-mail: naka@ynu.ac.jp

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When we use power devices in the electrical equipment incorporating Si devices, the heat removal is one of the most important issues because Si devices must be less than the temperature of 150°C not to affect the performance of Si devices and the equipment. Yamaguchi *et al.* have proposed a new scheme for cooling Si devices called the self-cooling devices [1]. However, it has yet to be shown that a comprehensive understanding of the self-cooling device is still lacking. To determine whether the self-cooling device remove the Joule heat from Si devices such as a power MOSFET under high current, we studied the temperature distribution measurement by using the infrared thermography. Figure 1 shows the temperature distribution of the upper side when the power MOSFET without n-type Si wafer generate the Joule heat ($R_{On}I^2=5.40W$, where $R_{On}=1.5m\Omega$), where the current of $I=60A$ flowed from the drain to the source. The temperature distribution in the upper side has a maximum at 41.4°C. On the other hand, it is clearly shown that the temperature distribution of the upper side shifts about 2°C to the low temperature when the power MOSFET with n-type Si wafer, i.e., the self-cooling device generate the Joule heat ($RI^2=9.00W$, where $R=2.5m\Omega$) as shown in Fig.2. The temperature distribution in the upper side has a maximum at 39.4°C. This fact indicates that the n-type Si wafer removes the heat from the upper side to the water cooled heatsink by both the Peltier effect due to the self-current of $I=60A$ ($|S|TI=12.4W$, where $|S|=688\mu V/K$ at $T=300K$) and the thermal conduction. These observations indicate that n-type Si wafer cools down the power MOSFET by using both the Peltier effect and the conventional thermal conduction. These results provide new insight that the self-cooling device is one of the efficient means to remove the heat from Si devices.

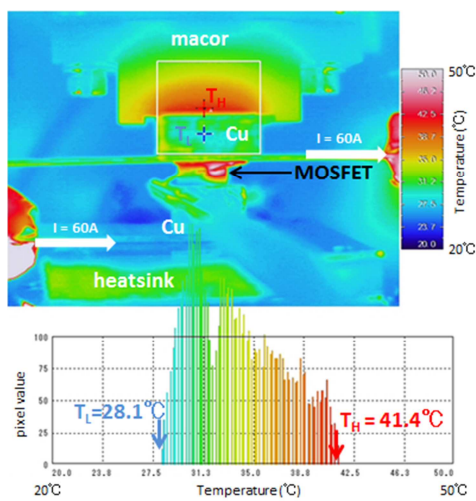


Fig.1 Temperature distribution (MOSFET only)

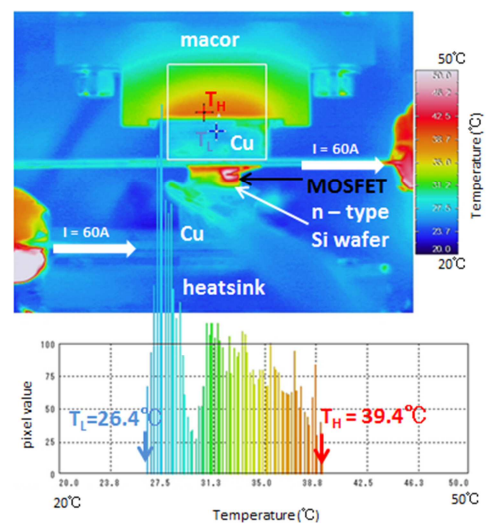


Fig.2 Temperature distribution (MOSFET + Si wafer)

References

- [1] S.Yamaguchi, Y.Okamoto, A.Yamamoto, and M.Hamabe: presented at 26th ICT2007.